PTO/SB/08A (08-00)

Please type a plus sign (+) inside this box → [+]

Approved for use through 10/31/2001. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 3

Complete if Known	
Application Number	10/618,237
Filing Date	July 11, 2003
First Named Inventor	Gang Zhang et al.
Group Art Unit	2825
Examiner Name	Not Yet Assigned
Attorney Docket Number	2879-030687

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, cite and/or country where published.	T[2]
BB	1	R. HARJANI, R.A. RUTENBAR and L.R. CARLEY, "OASYS: A Framework For Analog Circuit Synthesis", IEEE Transactions On Computer-Aided Design, Vol. 8, No. 12, pp. 1247-1266, (December 1989).	
	2	M.G.R. DEGRAUWE, O. NYS, E. DIJKSTRA, J. RIJMENANTS, S. BITZ, B.L.A.G. GOFFART, E.A. VITTOZ, S. CSERVENY, C. MEIXENBERGER, G. VAN DER STAPPEN, and H. J. OGUEY, "IDAC: An Interactive Design Tool For Analog CMOS Circuits", IEEE Journal Of Solid State Circuits, Vol. Sc-22, No. 6, pp. 1106-1116, (December 1987).	
	3	H.Y. KOH, C.H. SEQUIN and R.R. GRAY, "OPASYN: A Compiler For CMOS Operational Amplifiers", IEEE Transactions On Computer-Aided Design, Vol. 9, No. 2, pp. 113-125 (February 1990).	
	4	E. OCHOTTA, L.R. CARLEY and R.A. RUTENBAR, "Analog Circuit Synthesis For Large, Realistic Cells: Designing A Pipelined A/D Converter With ASTRX/OBLX", in Proc., IEEE Custom Integrated Circuit Conference, pp. 365-368, (1994).	
	5	R. PHELPS, M. KRASNICKI, R.A. RUTENBAR, L.R. CARLEY and J.R. HELLUMS, "A Case Study Of Synthesis For Industrial-Scale Analog IP: Redesign Of The Equalizer/Filter Frontend For An ADSL CODEC", ACM/IEEE Design Automation Conference, pp. 1-6 (June 2000).	
	6	G.G.E. GIELEN and R.A. RUTENBAR, "Computer-Aided Design Of Analog And Mixed-Signal Integrated Circuits", Proceedings Of The IEEE, Vol. 88, No.12, pp. 1825-1852 (December 2000).	
	7	J. RIJMENANTS, J.B. LITSIOS, T.R. SCHWARZ and M.G.R. DEGRAUWE, "ILAC: An Automated Layout Tool For Analog CMOS Circuits", IEEE Journal Of Solid State Circuits, Vol. 24, No. 2, pp. 417-425, (April 1989).	
	8	E. FELT, E. MALAVASI, E. CHARBON, R. TOTARO and A. SANGIOVANNI-VINCENTELLI, "Performance-Driven Compaction For Analog Integrated Circuits", IEEE 1993 Custom Integrated Circuits Conference, pp. 17.3.1-17.3.5, (1993).	
	9	U. CHOUDHURY and A. SANGIOVANNI-VICENTELLI, "Constraint Generation For Routing Analog Circuits", 27th ACM/IEEE Design Automation Conference, pp. 561-566, (June 1990).	
V	10	E. CHARBON, E. MALAVASI, U. CHOUDHURY, A. CASOTTO and A. SANGIOVANNI-VICENTELLI, "A Constraint-Driven Placement Methodology For Analog Integrated Circuits", IEEE 1992 Custom Integrated Circuits Conference, pp. 28.2.1-28.2.4, (May 1992).	

Examiner Signature	Brian Bowers	Date Considered	11/14/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Unique citation designation number. [2]See attached Kinds of U.S. Patent Documents. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

PTO/SB/08A (08-00)

Please type a plus sign (+) inside this box → [+]

Approved for use through 10/31/2001. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 2 of 3

Complete if Known	
Application Number	10/618,237
Filing Date	July 11, 2003
First Named Inventor	Gang Zhang et al.
Group Art Unit	2825
Examiner Name	~~Not Yet Assigned~~
Attorney Docket Number	2879-030687

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, cite and/or country where published.	T[2]
BB	11	E. CHARBON, E. MALAVASI, D. PANDINI and A. SANGIOVANNI-VINCENTELLI, "Imposing Tight Specifications On Analog IC's Through Simultaneous Placement And Module Optimization", IEEE 1994 Custom Integrated Circuits Conference, pp. 525-528, (May 1994).	
	12	E. CHARBON, G. HOLMLUND, A. SANGIOVANNI-VICENTELLI and B. DONECKER, "A Performance-Driven Router For RF And Microwave Analog Circuit Design", IEEE 1995 Custom Integrated Circuits Conference, pp. 383-386, (May 1995).	
	13	E. MALAVASI and A. SANGIOVANNI-VICENTELLI, "Area Routing For Analog Layout", IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 12, No. 8, pp. 1186-1197, (August 1993).	
	14	E. MALAVASI and A. SANGIOVANNI-VICENTELLI, "Dynamic Bound Generation For Constraint-Driven Routing", IEEE 1995 Custom Integrated Circuits Conference, pp. 477-480, (May 1995).	
	15	P. VANCORENLAND, G. VAN DER PLAS, M. STEYAERT, G. GIELEN, and W. SANSEN, "A Layout-Aware Synthesis Methodology For RF Circuits", 2001 IEEE, pp. 358-362, (2001).	
	16	K. LAMPAERT, G. GIELEN and W. SANSEN, "Direct Performance-Driven Placement Of Mismatch-sensitive Analog Circuits", 32nd ACM/IEEE Design Automation Conference, pp. 445-449, (June 1995).	
	17	B. ARSINTESCU, and R.H.J.M. OTTEN, "Constraints Space Management For The Layout Of Analog IC's", Proc. IEEE International Conference On Computer Aided Design (1996).	
	18	J.M. COHEN, D.J. GARROD, R.A. RUTENBAR and L.R. CARLEY, "KOAN/ANAGRAM II: New Tools For Device-Level Analog Placement And Routing", IEEE Journal Of Solid-State Circuits, Vol. 26, No. 3, pp. 330-342, (March 1991).	
	19	S. MITRA, S.K. NAG, R.A. RUTENBAR and L.R. CARLEY, "System-Level Routing Of Mixed-Signal ASICs IN WREN", Proc. IEEE Conference On Computer Aided Design, pp. 394-399, (November 1992).	
V	20	S. MITRA, R.A. RUTENBAR, L.R. CARLEY and D. J. ALLSTOT, "Substrate-Aware Mixed-Signal Macro-Cell Placement In WRIGHT", IEEE Journal Of Solid-State Circuits, Vol. 30, No. 3, pp. 269-278, (March 1995).	

Examiner Signature	Burton Bowen	Date Considered	11/14/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Unique citation designation number. [2]See attached Kinds of U.S. Patent Documents. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

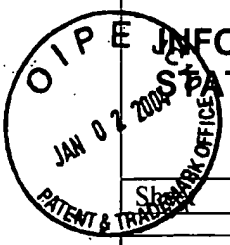
PTO/SB/08A (08-00)

Please type a plus sign (+) inside this box → [+]

Approved for use through 10/31/2001. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO



INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	3	of	3

Complete if Known	
Application Number	10/618,237
Filing Date	July 11, 2003
First Named Inventor	Gang Zhang et al.
Group Art Unit	2825
Examiner Name	~~Not Yet Assigned~~
Attorney Docket Number	2879-030687

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, cite and/or country where published.	T[2]
BB	21	G. ZHANG, A. DENGI, and L.R. CARLEY, "Automatic Synthesis Of A 2.1GHz SiGe Low Noise Amplifier", IEEE RFIC Symposium, pp. 1-4 (June 2002).	

Examiner Signature	Brian Bowan	Date Considered	11/14/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Unique citation designation number. [2]See attached Kinds of U.S. Patent Documents. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.